REMARKS

The following remarks are made in response to the Office Action mailed April 21, 2005. Claims 16 and 17 have been withdrawn from consideration. Claims 16 and 17 have been cancelled. Claims 1-15 were rejected. With this Response, claims 1, 6, and 7 have been amended. Claims 1-15 remain pending in the application and are presented for reconsideration and allowance.

Claim Rejections under 35 U.S.C. § 112

The Examiner rejected claims 7-15 under 35 U.S.C. § 112, second paragraph, for being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention.

The Examiner rejected claim 7 for insufficient antecedent basis for the limitation in the claim. Claim 7 recites the limitation "the edge sides."

With this Response, Applicants have amended claim 7 such that it now depends on claim 6. In this way, sufficient antecedent basis is provided for "the edge sides."

In view of the above, claims 7-15 are believed to be in form for allowance. Therefore, Applicants respectfully request the rejections to these claims under 35 U.S.C. § 112, second paragraph, be reconsidered, and the rejections be removed and these claims be allowed.

Claim Rejections under 35 U.S.C. § 102

The Examiner rejected claims 1-5 under 35 U.S.C. § 102(b) as being anticipated by Comette U.S. Patent No. 3,887,783. The Examiner cited Figures 1 and 2 in Comette, asserting that they disclose elements of claims 1-5.

Applicants respectfully disagree with the Examiner's apparent interpretation of the teachings of Comette. Specifically, the Examiner appears to be interpreting the tab strip 20 illustrated in Figures 1 and 2 of the Comette reference as being part of the semiconductor wafer. This is not correct. A "semiconductor water," as is well known in semiconductor device manufacturing, is understood as a wafer comprised of semiconductor material. Furthermore, a

"semiconductor chip" is semiconductor material with an integrated circuit structure and does not include the substrate in which it is mounted. In this way, tab strip 20 in the Comette reference cannot properly be considered part of the "semiconductor chip," as used in the present invention, and thus, the reference does not anticipate claim 1.

Applicants have amended claim 1 to further clarify the distinction between the present invention and such non-analogous art as Comette. The present invention has a semiconductor wafer comprising integrated circuits for semiconductor chips arranged in rows and columns on its wafer top side (see, page 2 of the specification, lines 2-3). The strip-type separating regions are arranged between the integrated circuits of the semiconductor chips (see, page 2 of the specification, lines 4-5). No such wafer having such arranged integrated circuit is disclosed in Comette. For this reason, it is believed the present invention allowable over the Comette reference, and this rejection should be removed.

Since claims 2-5 depend from claim 1, they are also similarly not anticipated.

The Examiner also rejected claims 1-5 under 35 U.S.C. § 102(b) as being anticipated by Thomas U.S. Patent No. 6,213,347. The Examiner cited Figures 7 and 8 of the Thomas reference, asserting that they disclose elements of claims 1-5.

As discussed above, amended claim 1 includes a semiconductor wafer comprising integrated circuits for semiconductor chips arranged in rows and columns on its wafer top side. The Thomas reference does not teach or suggest this. Instead, Thomas discloses a plurality of electronic components, each including a semiconductor 70 that is mounted on a substrate 71. As is apparent to one skilled in the art, the semiconductor chip does not include a substrate on which it is mounted. Consequently, the Thomas reference does not anticipate or suggest claim 1, and this rejection should be removed.

Since claims 2-5 depend from claim 1, they are also similarly not anticipated.

The Examiner also rejected claims 1-5 under 35 U.S.C. § 102(e) as being anticipated by Igarashi et al. U.S. Publication No. 2004/0169271. The Examiner asserts that Figures 1 and 2 of Igarashi disclose the elements of claim 1. Again, as amended, claim 1 includes a semiconductor wafer comprising integrated circuits for semiconductor chips arranged in rows and columns on

its wafer top side. Since semiconductor chip includes only the semiconductor material with the integrated structures and does not include the substrate on which it is mounted, nothing in Igarashi teaches or suggests the elements of claim 1, as amended. Consequently, this rejection should be removed.

Since claims 2-5 depend from claim 1, they are also similarly not anticipated.

The Examiner rejected claim 6 under 35 U.S.C. § 102(b) as being anticipated by Comette U.S. Patent No. 3,887,783. The Examiner cited Figures 1 and 2 in Comette, asserting that they disclose elements of claim 6.

Claim 6 has now been amended to further clarify that edge contacts are connected to electrodes of the integrated circuit via conductor tracks that are located on the top surface of the semiconductor chip. The Comette reference fails to teach or suggest conductor tracks on the top surface of the semiconductor chip. Consequently, this rejection should also be removed.

The Examiner rejected claim 6 under 35 U.S.C. § 102(e) as being anticipated by Igarashi et al. U.S. Publication No. 2004/0169271. The Examiner asserts that Figure 2 of Igarashi anticipates claim 6.

Again, as amended, claim 6 includes edge contacts that are connected to electrodes of the integrated circuit via conductor tracks that are located on the top surface of the semiconductor chip. Igarashi fails to disclose conductor tracks on a top surface of the semiconductor chip. Furthermore, the Examiner appears to assert that the edge sides of region 11 in Igarashi provide edge contacts. However, it is clear that regions 11 are conductor patterns and are not edge sides of the semiconductor chips 12. Consequently, in the region based on Igarashi should also be removed.

In view of the above, claims 1-15 are believed to be in form for allowance. Therefore, Applicants respectfully request rejections to these claims under 35 U.S.C. § 102(b) and (e) be reconsidered, and the rejections be removed and these claims be allowed.

CONCLUSION

In view of the above, Applicant respectfully submits that pending claims 1-15 are in form for allowance and are not taught or suggested by the cited references. Therefore, reconsideration and withdrawal of the rejections and allowance of claims 1-15 is respectfully requested.

No fees are required under 37 C.F.R. 1.16(b)(c). However, if such fees are required, the Patent Office is hereby authorized to charge Deposit Account No. 50-0471.

The Examiner is invited to contact the Applicant's representative at the below-listed telephone numbers to facilitate prosecution of this application.

Respectfully submitted,

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CERTIFICATE UNDER 37 C.F.R. 1.8: The undersigned hereby certifies that this paper or papers, as described herein, are being deposited in the United States Postal Service, as first class mail, in an envelope address to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this 21st day of July, 2005.

By
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